Network Infrastructure
Optical
Packet
Automation

Systems Integration
Turn-up & Test
Design & Optimize
Open Initiatives

WHY TEST OPTICS?

#1 Benchmark network performance
#2 Understand performance ambiguity
#3 Improve network roadmap

Optics and their interface circuitry, are critical components of next-gen architectures. Yet due to their high cost, manufacturing complexity, diverse form factors, flexible modulations, and precise orchestration, they carry a significant amount of performance ambiguity.

As an independent third-party test facility, Vayu Group gathers optics test data that would otherwise go undetected. Our test framework will provide data to your infrastructure team and improve their ability to:

A. Quantify OEM/ODM modules and components against MSAs and/or IEEE standards.

B. Pinpoint quality control issues, revealing where to install test stations and scripts for fault detection and problem resolution.

C. Drive component improvements with the OEM/ODM at factory or fab level.

D. Correlate anomalies in a production network with lab projections.

E. Build test scripts and in-house proprietary software for optics validation and characterization.

F. Define functional performance of optics and circuitry, including how hot to run your network.

G. Accurately project module failures for supply chain and lifecycle management.

H. Provide strategic data points for new design and systems development.

I. Target capex and opex decisions with greater clarity.

GENERAL SURVEY FRAMEWORK

We develop a testing framework to suit your signal structure, whether line-side transmission with multiple services or client transmissions with consistent signal. Our initial test framework assesses general categories and, through collaboration with your infrastructure team, we systematically narrow test parameters to survey performance in the following areas.

- Component evaluation: DSP, ROSA, TIA, DAC, EML, ITLA, and interfaces
- Module hardware and management: PCB, ESD, and temperature
- Firmware and software: command interface, module s/w and f/w integration
- Standards validation: MSA and IEEE compliance standards and format validation
- Production: function, throughput, signal integrity, and data path
- Vendor selection: evaluate modules based on RFP requirements
- Module integration: hardware and firmware with host and client

We develop a range of tests to quantify specific component or module performance. Each test series can be applied with varying degrees of depth and complexity as outlined below.

TEST FRAMEWORK

Optical Interface Tests

1. Center wavelength metric Tx and Rx
2. Power per lane and differential per lane
3. Extinction ratio or power of signal in separate positions
4. Side mode suppression ratio or amplitude differential
5. Amplitude differential ratio
6. Optical return loss ration at Tx and Rx
7. Receive sensitivity of dimmest signal
8. Receiver stressed recovery validation
9. Relative intensity noise parameters
10. Link budget tolerance and variation levels
11. BER of Tx
12. Transmitter dispersion penalty
13. Transmitter eye compliance with IEEE
14. Stress temperature, humidity, materials expansion/contraction
15. Port accuracy of pluggable
16. Receiver pluggable overload
17. Receiver jitter and wander tolerance
18. Transmitter average optical power
19. Latency test Tx

Validation of:

- Continuity with MSA
- Module layout and signal path functionality
- Traffic throughput, framer, and SerDes h/w and f/w
- Physical layer interface, signal integrity, clocking, and skew tolerance

20. Transmitter dispersion eye closure quaternary measurements
21. PAM4 transmitter signal level thickness
22. PAM4 transmitter linearity
23. Eye skew differentials
24. Central wavelength deviation
25. Duty cycle distortion pulse deviations
26. PAM4 transmitter separation mismatch ratio
27. Vertical eye closure penalty
28. Mask margin device
29. Eye crossing percentage
30. Spectral flatness Tx
31. Transmitter average optical power
32. Transmitter reflectance
33. Receiver reflectance
34. Maximum discrete reflectance
35. Laser bias current of transceiver
36. Module communication
37. EERPOM functions LOS assert level of receiver

Validation of:

- Ability to read off key performance
- Compatibility Ethernet, OTN, FlexO
- Behavior under impairments OSNR, bandwidth shaping, polarization
- Firmware stability and DSP coding
- Autonomous recovery time LOS

Electrical Interface Tests

38. Electrical stress test timing deviations
39. Electrical analysis transceiver module
40. Reset operations transceiver module
41. Transmitter interface specifications
42. Temperature exceed specifications
43. Voltage exceed specifications
44. Humidity exceed specifications
45. Current exceed specifications
46. Transmitter interface eye mask hit ratio
47. PAM4 transmitter linearity
48. Signal to noise distortion ratio receiver sensitivity
49. Differential output level voltage receiver of the transceiver module
50. Direct PAM4 analysis (simultaneous sampled signal)
51. NRZ and PAM4 transceiver receiver flexibility between modulations

Validation of:

- Electrical equalization host to module interface
- 3.3V at over 4A power requirements
- TIA and ADC range
- environmental stress

Systems Integration Tests

52. Integration L2/L3 BERT transitiver module
53. Alarm and error response on transceiver module
54. Interoperability and multi-vendor interconnection
55. 72 hours stress all lanes at edge of specifications
56. 7 day soak stress all lanes at edge of specifications

Validation of:

- Network to module integration
- OTN, FlexO, Ethernet compatibility
- Alarm and errors with corrective recovery procedures

Inspectional Tests:

57. Physical dimensions and materials specifications
58. Lens surface irregularities on transceiver module
59. Aging test and impact on transceiver module

Vendor Tests

60. Compatibility with third party components, switches, protocols
61. 400G FEC aware receiver versus FEC stripped
62. Optical receiver stress 100G LR4, ER4, SR4, CLR4, CWDM4, 4WDM
63. Jitter conformance N4917B stressed receiver
64. Error ratio analysis for PAM4
65. Digital threshold power continuity varying the eye pattern
66. PAM4 and NRZ time characterization interval
67. Power level characterization of 100G LR4, ER4, 4WDM transceiver
68. 100G Ethernet chip-to-chip and chip-to-module electrical
69. SerDes circuit characterization
70. Coherent Tx and Rx
71. Integrated coherent receiver
72. Stressed channel characterization NRZ and PAM4
73. C2C AUI input interference
74. FEC tolerance
75. Digital diagnostic monitoring of transceiver SNMP

Validation of:

- Multiple types of FEC usage
- FEC status / counters
- EVM
- Polarization tracking
- OS, management and control, conform to CMIS 4.0

TEST COMPLEXITIES

Despite the central role of optics, quantifiable optics data remains relatively inaccessible to most operators, who don't have the time nor equipment to extract it from the complex multi-domain stack. The ability to extract meaningful data is further complicated by imprecise orchestration, which greatly affects measurement accuracy and causes additional performance ambiguity.

- Software and firmware integration
- Management and control
- Materials management
- Higher modulation schemes
- Module development
- Multi-domain stack orchestration

The ability to test, measure, and narrow parameters is paramount to improve next-gen architectures. Vayu Group has a series of 1100 tests to quantify optics data and uncover meaningful performance metrics. Our tests provides a starting point on a challenging but necessary network optimization journey.

Contact info@vayugroup.net for additional information or consultation.